Zoran
Power Switch solution

July 2010
Leakage problem

- In deep sub-micron leakage becomes more dominant part of power consumption

- In 80nm process leakage can be responsible to 20-30% (50mA) of the total power consumption

Figures extracted from http://ixbtlabs.com/articles2/intel-65nm/
Solution

► Add a low-leakage switch on the Core power supply

► But Where to place it?
Solutions

► External switch
  ► Placing the switch on the system board, preferably as part of the DC-DC device

► Advantages
  ► Switch is part of the DC-DC converter
  ► Implemented using Analog process ➔ very low leakage

► Disadvantages
  ► Impossible to implement Fine power control
    ► Unless more than one DC-DC is used
  ► Long wake-up times
  ► Increase off chip device cost and area ➔ reducing compatibility
Solutions

Internal Switch

- Placing internal switch on Silicon as part of the device

Advantages

- Fine power delivery control is passable
- Reduce the number of on board devices
- In-house design
  - No dependency on external devices/manufactures

Disadvantages

- Increase chip area
- Switch implemented using Digital CMOS process still have large leakage problem
Solutions

▶ Internal Switch architectures
▶ Fine grain: control per cell
▶ Trade-off
▶ Enable fine grain power control
▶ Memory retention is possible
▶ Very large overhead increasing chip area
▶ Complicated IR/EM design

From “A Gate-Level Leakage Power Reduction Method for Ultra-Low-Power CMOS Circuits”
Solutions

- **Internal Switch architectures**
  - Coarse grain – Distributed: control the power rails creating “power islands”
    - Distributed: pad → mesh → PS → rails
  - Trade off
    - Fine power control can still be achieved
    - Memory retention is possible
    - Complicated IR/EM design
    - Lower area cost
Solutions

► Internal Switch architectures
  ► Very Coarse grain – Ring: control the power of the entire mesh
    ► Ring: pad → PS → mesh → rails
  ► Trade off
    ► Very small area cost
    ► Simple IR/EM design
    ► No memory retention
      ► Partial data retention is possible by increasing the Sleep logic section
    ► Long wake-up time
Common Implementation

- Common implementation is using MTCMOS (Multi Threshold CMOS process)
  - HVT CMOS transistor are used as power switches
  - The leakage is reduced by 60-70%
  - Solution is supported by major FAB, such as TSMC
  - For Very Coarse and Corse grain solutions
Zoran Power Switch

- No or negligible Leakage
- Internal Very coarse grain (Ring) methodology architecture
- Single supply (1.0V Core voltage)
- Core logic divided
  - Sleep/Standby logic
    - Controlling the power switches wake-up and shut-down sequences
    - Very small, less than 1% of total Core area
  - Chip Core
    - No memory retention
      - Requires reset cycle to wake up properly
Zoran Power Switch – initial solution

- Power switch was implemented using IO PMOS transistors which have very low leakage (<10pA/um)
- Switches the VDD ring
  - Easier block all leakage paths
- Requires a control signal of 1.0V
  - Available all the time
Zoran Power Switch – initial solution

► Trade offs
  ► Lower leakage
  ► Area cost
    ► Large W/L ratio needed to compensate for the IO PMOS low mobility
  ► Simple IR drop verification
    ► Switch can be treated as Resistor
  ► Wake up (performance)
    ► No data retention
    ► Relatively longer wake up time
    ► Rush current
      ► Peak IR drop
Zoran Power Switch – 2nd generation PS

- Power switch implemented using IO NMOS transistor
  - 3 times higher mobility
- Trade off
  - Smaller area (compared to previous solution)
    - Enables more flexible and efficient floorplan

![Zoran NMOS PS](image)

**Width = ~120um**

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**Zoran PMOS PS**

**Width = ~1200 um**
Zoran Power Switch – 2\textsuperscript{nd} generation PS
Zoran Power Switch – 2nd generation PS

► Trade off (cont.)
  ► Timing – faster wake-up time
    ► Smaller gate area → lower capacitance
  ► Higher gate voltage required
    ► To achieve better IR drop and reduce the chip area across the switch:
      ► $V_{GATE} > 2.3V$
        ► Requires an external 2.7/3.3V active supply during operation
        ► Or another HV supply source
# Power Switch – Summary

<table>
<thead>
<tr>
<th>Based on Approach5</th>
<th>Zoran NMOS PS</th>
<th>Zoran PMOS PS</th>
<th><strong>MTCMOS</strong>&lt;sup&gt;*&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>distributed current (300mA)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10mv</td>
</tr>
<tr>
<td>Area %</td>
<td>1.90%</td>
<td>5.67%</td>
<td>0.18%</td>
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<tr>
<td>Leakage mW TC (HVT)</td>
<td>0.00008</td>
<td>0.00006</td>
<td>0.005</td>
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<tr>
<td>Leakage mW ML (HVT)</td>
<td>0.02</td>
<td>0.05</td>
<td>0.558</td>
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</tbody>
</table>

- Zoran solution reduce leakage by >500 compared to conventional solution with 10 times the area cost

* Based on TSMC MTCMOS cells, single switch on VDD
Voltage Multiplier – Motivation

► For proper operation of the selected Power switch architecture we need to have $V_{\text{GATE}} > 2.3\text{V}$

► To avoid the requirement of an always-on 3.3V supply we use a voltage multiplier
Voltage Multiplier – Architecture

- There are several well known voltage multipliers architectures:
  - Vilard, Dickson, etc.
- We selected to use Clock booster with PMOS switch
Voltage Multiplier – Architecture

► To reach the desired voltage level (>2.3V) we used two stage connected serially, the clock required was generated using a local RC oscillator.
Voltage Multiplier – Architecture

Trade offs

- Simple stage design
- can be implemented using digital CMOS process
  - No deep-Nwell CMOS are used
- Low area
  - Very small peripheral circuits, simple switches
- Fast wake-up
  - Small capacitor
- Medium power efficiency
  - Not an issue - no current load once we reach target voltage
Silicon results – Power switch

- Total leakage during standby is <0.2mW at max leakage corner
- Power switch IR drop <5mV for $V_G > 2.3V$
## Silicon results – Voltage multiplier

- A single Voltage multiplier was used to drive 100 Power switches (Full chip)
- Voltage multiplier output voltage

<table>
<thead>
<tr>
<th>1st stage</th>
<th>2nd stage (output)</th>
<th>Output Voltage</th>
<th>Voltage gain</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td>0.95V</td>
<td>1.05V</td>
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<tr>
<td>FF</td>
<td>1.70</td>
<td>1.86</td>
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<tr>
<td>FS</td>
<td>1.71</td>
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<tr>
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<td>1.88</td>
<td>2.04</td>
</tr>
<tr>
<td>SF</td>
<td>1.72</td>
<td>1.88</td>
<td>2.04</td>
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<tr>
<td>SS</td>
<td>1.75</td>
<td>1.92</td>
<td>2.08</td>
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<tr>
<td><strong>Average</strong></td>
<td><strong>1.72</strong></td>
<td><strong>1.88</strong></td>
<td><strong>2.04</strong></td>
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<tr>
<td>FF</td>
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<tr>
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<tr>
<td><strong>Average</strong></td>
<td><strong>2.45</strong></td>
<td><strong>2.64</strong></td>
<td><strong>2.76</strong></td>
</tr>
</tbody>
</table>
Innovation

► Using IO CMOS in Power Switch in order to reduce switch static leakage
► Using Voltage Multiplier to get single supply solution
Summary

- **Static power consumption reduced by a factor of >500 vs. common architectures**
  - Single Power Switch leakage 1uW
    - Due to the usage of IO CMOS rather than HVT CMOS power switch (MTCMOS)
  - Voltage multiplier leakage 5uW

- **Minor area cost**
  - Voltage multiplier 32ku²
  - Single Power switch 4.8ku²

- **No increase in Dynamic power consumption**
  - Voltage multiplier <0.3mW

- **Single supply solution**

- **No or minor impact on physical design flow**
  - Power switch modeled as resistor for IR drop verification
Silicon Proven – LG Viewty
Thank You