REAL TIME POWER DELIVERY MANAGEMENT THROUGH SW-HW SYMBIOSIS

Michael Zelikson, Vjekoslav Svilan
Agenda

- Power Saving through Dynamic Voltage Scaling
- Dynamic Voltage Scaling and Integrated VRs
- Mitigation of transient response related droop
Voltage budget - breakdown

- Programmed voltage at VR
- VR2gate drop ($I_{CC@actual} \times LL_{total}$)
- Part of reliability & VR GBs
- $V_{actual}(F, stress)@gate$
- Actual overvoltage@$gate$, $30 \rightarrow 90 \text{ mV}$
Dynamic Power Gating (Zelikson et al, ICTC 2010) enables power savings during C0 state

- Reduce current consumption in real time by absorbing Tx overvoltage on power gate with controllable resistance ➔ saves current, not voltage
- Limited by unpredictability of current consumption

Code Morphing Software, CMS, is capable of upfront estimation of max or average currents

Combination of dynamic power gating with CMS enables power management in active machine state
Binary Translation Based Architecture

IA (000) Processor

Memory
x86 data
x86 instr

I Cache
x86 instr

x86 decoders

Out-of-Order Execution Engine

Data Cache
x86 data

In Order Processing

Memory
x86 instr
x86 data

UOP instr

ROM

I Cache
UOP instr

Dynamic Binary Translator (CMS)
• x86 to UOP decoding
• Rescheduling UOPs out of order
• Optimization: fewer instructions to run

UOPs

UOPs (mISA)

Data Cache
x86 data

In-Order Execution Engine
Divide a core into regions corresponding to CMS pipes (ALU, VPU, MEM, etc)

Define \( n \) activity grades: zero (=idle) to MAX (per a region)

CMS maps current pipe activity into activity grades scale

CMS calculates correspondent \( R_{\text{EPG}} \) using PCU data

CMS alarms a change in a pipe activity & sets new \( R_{\text{EPG}} \) value

\[
R_{\text{EPG}}^{\text{pipe}_i} = \frac{V_{\text{CCU}} - V_{\text{target}}}{I_{\text{leak}}^{\text{pipe}_i}(T, V_{\text{target}}) + C_{\text{real}}^{\text{pipe}_i} V_{\text{target}}^f} - R_{\text{grid}}^{\text{pipe}_i}
\]

\[
R_{\text{EPG}}^{\text{pipe}_i}[t_n] \rightarrow R_{\text{EPG}}^{\text{pipe}_i}[\text{virus}] \rightarrow R_{\text{EPG}}^{\text{pipe}_i}[t_{n+1}]
\]

Enables gate voltage control with ~10 ns resolution
CMS Power Estimation

- During translation scheduling, estimate worst case power likely to be used by that translation and assign average activity grade (#of grades TBD) either per translation, or even more fine grained, per pipe in the translation.
- Add grade information to the beginning of the translation in the form of MSR Write or similar so that EPG control can use it.
- In case of anticipated power surge, release all EPGs to a minimal resistance value.
# Dynamic Voltage Scaling ROI – Example

<table>
<thead>
<tr>
<th>Entity</th>
<th>Value</th>
<th>Power virus</th>
<th>App w/o PG</th>
<th>App w PG</th>
</tr>
</thead>
<tbody>
<tr>
<td>VID [mV]</td>
<td>1035</td>
<td>2.4</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>GB [mV]</td>
<td>50</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Freq [GHz]</td>
<td>4.65</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LL ext [mΩ]</td>
<td>3.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LL int [mΩ]</td>
<td>1.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PG res [mΩ]</td>
<td>0.7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vgate [mV]</td>
<td>900</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Cdyn [nF]</td>
<td></td>
<td>2.4</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Active/Leakage Current [A]</td>
<td>10.04/3</td>
<td>2.20/3.5</td>
<td>2.10/3</td>
<td></td>
</tr>
<tr>
<td>LL ext+int Voltage Drop [mV]</td>
<td>70</td>
<td>30</td>
<td>27</td>
<td></td>
</tr>
<tr>
<td>PG Resistance Multiplier</td>
<td>14</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PG Voltage Drop [mV]</td>
<td>10</td>
<td>5</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>Vgate_over-voltage[mV]</td>
<td>0</td>
<td>45</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Power [W]</td>
<td>13.35</td>
<td>5.83</td>
<td>5.22</td>
<td></td>
</tr>
</tbody>
</table>

% Power savings (for a given application) | 10.4% |

Reaches >10% power savings (+factor idle state gain)
Given: $V_{\text{gate}} \sim V_{\text{bump}} = 0.8 \text{ V}$, $I_{\text{CC max}} = 7 \text{ A}$ (assume 5 GHz and 1.75 nF $C_{\text{dyn}}$)
$I_{\text{leak}} = 3 \text{ A}$.

Longrun sets new $(V, f) = (0.5 \text{ V}, 1.5 \text{ GHz})$.

- No change in EPG resistance $\rightarrow I_{\text{leak}} = 3 \text{ A}$, $I_{\text{CC max}} = 7 \times 1.5 / 5 = 2.1 \text{ A} \rightarrow P = 0.8 \times 5.1 = 4.08 \text{ W}$
- High-R EPG $\rightarrow V_{\text{gate}} = 0.55 \text{ V}$ $\rightarrow I_{\text{leak}} = 1.4 \text{ A}$, $I_{\text{CC max}} = 7 \times 1.5 / 5 \times 0.55 / 0.8 = 1.44 \text{ A} \rightarrow P = 0.8 \times 2.84 = 2.27 \text{ W}$
- To achieve 250 mV drop on EPG one needs: $R_{\text{EPG}} = 250 / 2.84 = 88 \text{ m} \Omega$, which is 2.27% of original $Z_{\text{EPG}}$

Now CMS sets $C_{\text{dyn}} = 0.85$

- $I_{\text{CC}} = 1.44 \times 0.85 / 1.75 = 0.7 \text{ A} \rightarrow \text{New } R_{\text{EPG}}$ for same $V_{\text{gate}} = 250 \text{ mV} / (1.4 + 0.7) = 119 \text{ m} \Omega$.
  $\rightarrow$ need to switch off additional 0.6% of original $Z_{\text{EPG}}$ (~14,000 $\mu$m)
- Non-trivial control and routing problem – need to enable very fine resolution over wide $R_{\text{EPG}}$ range. Probably exponential scale is useful
Can mitigate hidden GB due to a.c. load line effects

 Makes unification of domains more efficient
  - Minimal power penalty even if some $\Delta V_{ID}$ exists
  - Positive ROI, even considering PG additional resistance

 Partial ripple cancelation is feasible

Frequently pays off, even together with integrated VR
Current step $\Rightarrow V_{CC}$ droop $\Rightarrow$ Higher GB
- More significant for zero d.c. load line design
CMS can predict big current steps $\sim$5ns upfront
IVR can use such CMS early warning to raise Vout prior to the transient

Integration of CMS data into FIVR control scheme enables reduction of transient response related GB
Regular noise $< 80 \text{ mV}$

Transient Droop e.g. $150 \text{ mV}$

Forced, all phases together, $V_{CC \text{ pre-charge}} \leq 100 \text{ mV}$

IVR PWM controls schedule is back to normal, i.e. interleaved, mode

High IVR BW enables timely tuning of $V_{CC}$, effectively mitigating transient droop

Principle scheme only. Not part of a standard IVR design
Combination of dynamic power gating with CMS enables power management in active machine state

- Enables gate voltage control with ~10 ns resolution
- Provides >10% power savings (+factor idle state gain)
- Frequently pays off, even together with integrated VR

Integration of CMS data into IVR control scheme enables reduction of transient response related GB

- High IVR BW enables timely tuning of VCC, effectively cancelling transient droop