Distributed On-Chip Power Regulators and Decoupling Capacitors

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Delivering High Quality Power On-Chip
Flow of Presentation

- Power delivery: yesterday, today, and tomorrow
- Heterogeneous power delivery management
- Future research
- Summary
Flow of Presentation

- Power delivery: yesterday, today, and tomorrow
  - From power plant to integrated circuit
  - Power delivery architectures
- Heterogeneous power delivery management
- Future research
- Summary
Electricity – From Power Plant to House

Power plant

Step-up transformer

Transmission lines

Step-down transformer

155 kV – 765 kV direct current (DC) or AC

<10 kV

Local distribution lines

155 kV – 765 kV

120 V alternating current (AC)

120 V
Electricity – From House to Computer Board

Intel Skulltrail motherboard – D5400XS - 2009
Electricity – From Board to Integrated Circuit
Toshiba HD decoding chip – 2011

25 power domains

(2)-(11) Video/Audio multiprocessor
(17) Full-HD video
  H.264 Codec engine
(19) 3D/2D graphics engine
(20)-(22) ARM processor
(15) Camera I/F
(14) Display I/F
(16) Image composition
(12) JPEG/Video scaling
(1)(13)(18)(23) Main bus
(24) Control bus /
  Peripheral I/F
(25) I/O

(a) SCS-DRAM I/F
Electricity – From Board to Integrated Circuit
Samsung Exynos 4 Quad Core – 2012

- Quad core application processor
  - 32 nm
  - High-k metal gate
  - Over 1.4 GHz per core

- Separate power management IC
  - Nine buck converters
  - 28 LDOs

- Dynamic voltage and frequency scaling (DVFS)
  - 6.25 mV step size
Power Management – Adaptive Power Supply

- Centralized power management controller
- Hybrid power supply
  - Buck converter and switched capacitor regulators
- Suffers from low power efficiency
  - 41% to 93%
  - Switched capacitor regulator

Dynamic Voltage Scaling (DVS)

- On-chip power management area
  - 0.36 mm²
- Centralized control
  - Far from the load
    - Slow transient response

- Power management with low power PWM and high efficiency pre-regulator
  - Off-chip inductor (4.7 µH) for the pre-regulator

Software Controlled Power Management – Intel SpeedStep Technology

- Software controlled power management
  - Centralized hardware
- Voltage ramp rates are controlled
- Dynamically change frequency of PLLs by changing input voltage

Full On-Chip Power Management – 65 nm CMOS Cellular Handset Chip

- Buck converter with ten LDOs
  - ~ 0.9 mm²
- 85% power efficiency
- Centralized power management and power supplies
  - Far from load circuits
    - Higher power noise

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- Power delivery: yesterday, today, and tomorrow
  - From power plant to integrated circuit
    - Power delivery architectures
      - Background and issues
        - Separation of power conversion and regulation
  - Heterogeneous power delivery management
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  - Summary
Active Power Supplies – Circuit Examples

Power supply (noisy and high)

Linear

Power converter/regulator

Switched Capacitor (SC)

Power supply (stable and low)

Switching (SMPS)

LDO

Series-parallel

Buck
# Switching vs. Linear Power Supplies

<table>
<thead>
<tr>
<th></th>
<th>SMPS / SC</th>
<th>Linear</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Area</strong></td>
<td>• Medium for SC</td>
<td><strong>Small</strong></td>
</tr>
<tr>
<td></td>
<td>• Large for SMPS</td>
<td>• Increasing with current load</td>
</tr>
<tr>
<td><strong>Response time</strong></td>
<td>Slow</td>
<td><strong>Fast</strong></td>
</tr>
<tr>
<td><strong>Step-up/ step-down</strong></td>
<td><strong>Both</strong></td>
<td><strong>Step-down</strong></td>
</tr>
<tr>
<td><strong>Power efficiency</strong></td>
<td><strong>Good</strong></td>
<td>Limited to $V_{OUT} / V_N$</td>
</tr>
<tr>
<td></td>
<td>• Drops with on-chip integration</td>
<td>• $V_{OUT} - V_N$ should be minimized</td>
</tr>
<tr>
<td></td>
<td>• Drops with current load</td>
<td></td>
</tr>
<tr>
<td><strong>Voltage regulation</strong></td>
<td>• <strong>Good</strong> in SMPS</td>
<td><strong>Good</strong></td>
</tr>
<tr>
<td></td>
<td>• Poor in SC</td>
<td></td>
</tr>
</tbody>
</table>
Off-Chip Power Delivery – Past

- Off-chip power converters
  - Parasitic effects
    - Resistive IR drop
    - Inductive L di/dt noise
  - High number of I/O pins
On-Chip Power Delivery – Present

- **On-chip power converters**
  - Parasitic effects eliminated
  - Smaller converters required
### Active vs. Passive Power Supplies

<table>
<thead>
<tr>
<th></th>
<th>On-chip power converters and regulators</th>
<th>On-chip decoupling capacitors</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Area</strong></td>
<td>Greater area requirement</td>
<td>Smaller area requirement</td>
</tr>
<tr>
<td><strong>Response time</strong></td>
<td>Slower response</td>
<td>Faster response</td>
</tr>
<tr>
<td><strong>Power efficiency</strong></td>
<td>Limited efficiency due to the active devices and parasitic impedances</td>
<td>Power loss only due to parasitic impedances</td>
</tr>
<tr>
<td><strong>Maximum supplied current</strong></td>
<td>High</td>
<td>Limited to the size of the capacitor. Decay and recharge rate of the capacitor should be considered</td>
</tr>
</tbody>
</table>

- Exploit distinctive properties of decoupling capacitors and power supplies
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    - Design complexity
    - Design solutions
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On-chip power delivery is not one-dimensional

- Highly complicated power delivery system
  - Off-chip/in-package power converters
  - On-chip power regulators and decoupling capacitors

- Power noise analysis
  - Computationally complex
  - Significant memory requirement

Interactions of Power Supplies and Power Grid

Architectural interactions within off-chip and on-chip power supplies

LDO
Decap
Load

Physical interactions within on-chip power supplies and power grid

Off-chip power converters
I/O interface
Distributed on-chip LDOs
Voltage islands

Off-chip
On-chip

UNIVERSITY of ROCHESTER
Physical Design Complexity
Distribution of Regulators and Decaps with On-Chip Loads

- Several power distribution networks
- Hundreds of on-chip linear regulators
- Thousands of decoupling capacitors
- Billions of load circuits
Architectural Clustering of Power Supplies

- Tens of off-chip switching converters
- Hundreds of on-chip linear regulators
- Multiple power grids
- Billions of load circuits

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  - Design solutions
- Future research
- Summary
Delivering power to complex ICs is a fundamental bottleneck.

**Models**
- Closed-form expressions for effective power grid resistance

**Algorithms**
- Fast algorithms for power grid analysis

**Com-design methodology**
- Off-chip converters
- On-chip regulators
- Decoupling capacitors

**Circuits**
- Ultra-small point-of-load voltage regulator

**Architecture**
- Topologies for on-chip and off-chip co-design of power supplies

**Considering**
- Power efficiency
- High regulation (low noise)
- 3-D integration
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Active Filter Based Converter

- Rochester, Eastman Kodak, and TSMC
- 110 nm CMOS technology
- Voltage reference is replaced with active filter
  - Simple design
  - Low quiescent current
- Ultra-small voltage regulator
  - 0.015 mm$^2$ on-chip area
  - Suitable for on-chip distribution
- Fast response time

![Diagram showing an op-amp with active filter connected]
Active Filter Based Converter - Feedback

- Feedback within active filter structure
  - Fast transient response to changes in load
    - Similar to LDO
- Effective regulation of output voltage
  - Small changes in supply voltage
    - Sharp output load transients
Five different test circuits have been fabricated

- Three circuits with internal PWM module to provide input signal
- Two circuits with input signals supplied from off-chip signal generator
## Performance Summary

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Buck</td>
<td>LDO</td>
<td>LDO</td>
<td>LDO</td>
<td>LDO</td>
<td>LDO</td>
<td>SC</td>
<td>SC</td>
<td>Hybrid</td>
</tr>
<tr>
<td>Technology [nm]</td>
<td>80</td>
<td>500</td>
<td>90</td>
<td>350</td>
<td>350</td>
<td>90</td>
<td>45</td>
<td>32</td>
<td>110</td>
</tr>
<tr>
<td>Response time [ns]</td>
<td>87$^a$</td>
<td>150,000</td>
<td>0.654$^b$</td>
<td>270</td>
<td>300</td>
<td>3000-5000</td>
<td>120-1200</td>
<td>N/A</td>
<td>72-192</td>
</tr>
<tr>
<td>On-chip area [mm$^2$]</td>
<td>12.6</td>
<td>1</td>
<td>0.098</td>
<td>0.264</td>
<td>0.045$^c$</td>
<td>0.019</td>
<td>0.16</td>
<td>0.374</td>
<td>0.015</td>
</tr>
<tr>
<td>Output voltage [V]</td>
<td>0.9</td>
<td>2-3.6</td>
<td>0.9</td>
<td>1.8-3.5</td>
<td>1</td>
<td>0.5-1</td>
<td>0.8-1</td>
<td>0.66-1.33</td>
<td>0.9</td>
</tr>
<tr>
<td>Input voltage [V]</td>
<td>1.2</td>
<td>5</td>
<td>1.2</td>
<td>2-5.5</td>
<td>1.2</td>
<td>0.75-1.2</td>
<td>N/A</td>
<td>N/A</td>
<td>1.8</td>
</tr>
<tr>
<td>Maximum current [mA]</td>
<td>9500</td>
<td>300</td>
<td>100</td>
<td>200</td>
<td>50</td>
<td>100</td>
<td>8</td>
<td>205</td>
<td>89</td>
</tr>
<tr>
<td>Maximum current efficiency</td>
<td>N/A</td>
<td>99.8</td>
<td>94</td>
<td>99.8</td>
<td>99.8</td>
<td>99.9</td>
<td>N/A</td>
<td>N/A</td>
<td>99.5</td>
</tr>
<tr>
<td>$\Delta V_{out}$ [mV]</td>
<td>100</td>
<td>300</td>
<td>90</td>
<td>54</td>
<td>180</td>
<td>114</td>
<td>N/A</td>
<td>N/A</td>
<td>44</td>
</tr>
<tr>
<td>Quiescent current [mA]</td>
<td>N/A</td>
<td>10.750</td>
<td>6</td>
<td>0.02-0.34</td>
<td>0.095</td>
<td>0.008</td>
<td>N/A</td>
<td>N/A</td>
<td>0.38</td>
</tr>
<tr>
<td>Load regulation [mV/mA]</td>
<td>0.014$^a$</td>
<td>0.5</td>
<td>1.8</td>
<td>0.27</td>
<td>0.28</td>
<td>0.1</td>
<td>N/A</td>
<td>N/A</td>
<td>0.67</td>
</tr>
<tr>
<td>Transition time [ns]</td>
<td>N/A</td>
<td>N/A</td>
<td>0.1</td>
<td>100</td>
<td>–150</td>
<td>100</td>
<td>N/A</td>
<td>N/A</td>
<td>70</td>
</tr>
<tr>
<td>Transition time ratio ($R$)</td>
<td>N/A</td>
<td>N/A</td>
<td>1</td>
<td>1000</td>
<td>1500</td>
<td>1000</td>
<td>N/A</td>
<td>N/A</td>
<td>700</td>
</tr>
<tr>
<td>FOM$<em>1$=$K\left(\frac{\Delta V</em>{out}}{\Delta I_{out}}\right)^2 \cdot R \cdot A$</td>
<td>N/A</td>
<td>N/A</td>
<td>0.029$^b$</td>
<td>6.544</td>
<td>6.926$^c$</td>
<td>0.893</td>
<td>N/A</td>
<td>N/A</td>
<td>0.518</td>
</tr>
<tr>
<td>FOM$<em>2$=$K\left(\frac{\Delta V</em>{out}}{\Delta I_{out}}\right) \cdot \frac{R \cdot A}{T}$</td>
<td>N/A</td>
<td>N/A</td>
<td>3.6$^b$</td>
<td>53.4</td>
<td>56.5$^c$</td>
<td>110.2</td>
<td>N/A</td>
<td>N/A</td>
<td>42.8</td>
</tr>
</tbody>
</table>

$^a$Simulation results (not experimental data).

$^b$Mathematical analysis (not experimental data).

$^c$An off-chip capacitor of 1 nF to 10 μF is required.

Proposed regulator provides smallest **area**, fast **response** time, and low **quiescent current**


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    - Circuits
  - Models
    - Algorithms
    - Architecture
- Future research
- Summary
Effective Resistance Model

- Infinite semi-uniform two layer mesh
- Models power or ground network
- Effective resistance between arbitrary points within power grid
- IR drop analysis

**Exact solution**

\[ R_{x,y} = \frac{k r}{\pi} \int_{0}^{\pi} \frac{2 - e^{-|x|\alpha \cos \beta}}{\sinh \alpha} d\beta \]

**Asymptotic solution**

\[ R_{x,y}/r = \frac{\sqrt{k}}{2\pi} [\ln(x^2 + ky^2) + 3.44388] \\
- 0.033425k - 0.0629k(k-1) \text{ for } k \to 1 \]

Physical separation affects current supplied from
- Power supplies
- Decoupling capacitors

\[ i_{pl} = \left( R_{pl} + L_{pl} \frac{dV_c(t)}{dt} \right) - CR_{vd} \frac{dV_c(t)}{dt} - CL_{vd} \frac{d^2V_c(t)}{dt^2} \]

\[ i_{dl} = \frac{R_{vd} + R_{dl} + (L_{vd} + R_{dl}) \frac{dV_c(t)}{dt}}{R_{vd} + R_{dl} + (L_{vd} + R_{dl})} \]
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Fast Algorithms for Power Grid Synthesis

- Efficient algorithms to estimate IR voltage drops
- Significantly faster than existing techniques
- Non-iterative

\[ IR_{\text{node}} = \frac{1}{2} \sum_{i=1}^{m} \left[ I_{\text{load}}(i) \cdot (R_{sn} + R_{sl} - R_{nl}) \right] - \frac{1}{2} \sum_{i=2}^{n} \left[ I_{\text{supply}}(i) \cdot (R_{sn} + R_{sl} - R_{nl}) \right] \]


Where should power supplies and decoupling capacitors be placed?

Characteristics of decoupling capacitors and power supplies
- Spatial location
- Output impedance
  - Response time
- Maximum current

Characteristics of load circuits
- Spatial location
- Current demand

Characteristics of power network
- Parasitic impedances

- ISPD benchmark circuit
  - Superblue18
  - 483,452 individual blocks
- Power grid
  - ~ 400 horizontal lines
  - ~ 380 vertical lines

Benchmark Circuits – SuperBlue5

Map of voltage drops for superblue5

- Smaller voltage drop with distributed power delivery system

<table>
<thead>
<tr>
<th>Case</th>
<th># of PS</th>
<th># of Decaps</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Case 2</td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>Case 3</td>
<td>3</td>
<td>10</td>
</tr>
<tr>
<td>Case 4</td>
<td>3</td>
<td>20</td>
</tr>
<tr>
<td>Case 5</td>
<td>20</td>
<td>32</td>
</tr>
</tbody>
</table>

- # of blocks: 95,041
- Power grid size: 774 X 713
- # of nodes in the power grid: 551,862
Benchmark Circuits – SuperBlue10

Map of voltage drops for superblue10
  - Smaller voltage drop with distributed power delivery system

<table>
<thead>
<tr>
<th></th>
<th># of blocks</th>
<th>Power grid size</th>
<th># of nodes in the power grid</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>1</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Case 2</td>
<td>1</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Case 3</td>
<td>3</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Case 4</td>
<td>3</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>Case 5</td>
<td>20</td>
<td>32</td>
<td>32</td>
</tr>
</tbody>
</table>
Map of voltage drops for superblue12

- Smaller voltage drop with distributed power delivery system
Maps of voltage drops for superblue18

- Smaller voltage drop with distributed power delivery system

<table>
<thead>
<tr>
<th># of blocks</th>
<th>Power grid size</th>
<th># of nodes in the power grid</th>
</tr>
</thead>
<tbody>
<tr>
<td>41,047</td>
<td>381 X 404</td>
<td>153,924</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Case</th>
<th># of PS</th>
<th># of Decaps</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>10</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
<td>20</td>
</tr>
<tr>
<td>5</td>
<td>20</td>
<td>32</td>
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</tbody>
</table>
Distributed Power Delivery

<table>
<thead>
<tr>
<th></th>
<th>One power supply</th>
<th>One power supply</th>
<th>Three power supplies</th>
<th>Three power supplies</th>
<th>20 power supplies</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Two decaps</td>
<td>Ten decaps</td>
<td>Ten decaps</td>
<td>20 decaps</td>
<td>32 decaps</td>
</tr>
<tr>
<td>Maximum voltage drop</td>
<td>163 mV</td>
<td>130 mV</td>
<td>115 mV</td>
<td>73 mV</td>
<td>100 mV</td>
</tr>
<tr>
<td>Average voltage drop</td>
<td>134 mV</td>
<td>133 mV</td>
<td>106 mV</td>
<td>81 mV</td>
<td>98 mV</td>
</tr>
<tr>
<td>Maximum voltage drop</td>
<td>122 mV</td>
<td>106 mV</td>
<td>106 mV</td>
<td>81 mV</td>
<td>98 mV</td>
</tr>
<tr>
<td>Average voltage drop</td>
<td>73 mV</td>
<td>81 mV</td>
<td>81 mV</td>
<td>72 mV</td>
<td>72 mV</td>
</tr>
</tbody>
</table>

Maximum voltage drop decreases significantly with distributed power delivery.

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Objective

- Maximize power efficiency of system
- Satisfy on-chip area constraints

Design criteria

- Number of off-chip SMPS
- Number of POL LDOs
- Clusters of LDOs within SMPS
  - Choice of output voltage levels for SMPS converters

Off-Chip Factors in Heterogeneous Power System

Power Efficiency vs. Number of SMPS converters

- **Single off-chip SMPS**
  - 68% efficiency

- **Three off-chip SMPS**
  - 93% efficiency

![Diagram showing power loss and efficiency for single and three off-chip SMPS converters.](image)
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Delivering power to complex ICs is a fundamental bottleneck.

**Summary**

**Models**
- Closed-form expressions for effective power grid resistance

**Algorithms**
- Fast algorithms for power grid analysis

**Circuits**
- Ultra-small point-of-load voltage regulator

**Co-design methodology**
- Power delivery on-chip
  - Circuits
  - Models
  - Architecture
- Power supply distribution on-chip
  - Circuits
  - Models
  - Algorithms

**Architecture**
- Topologies for on-chip and off-chip co-design of power supplies
Power Management – Cross-Field Research

Optimization techniques
- Computational geometry
- Operations research

Interconnect evolution
- Interconnect complexity
- Bus signaling
- Network-on-chip paradigm
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Summary
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- **Models**
  - Closed-form expressions for effective power grid resistance

- **Algorithms**
  - Fast algorithms for power grid analysis

- **Circuits**
  - Ultra-small point-of-load voltage regulator

- **Co-design methodology**
  - Off-chip converters
  - On-chip regulators
  - Decoupling capacitors

- **considering**
  - Power efficiency
  - High regulation (low noise)
  - 3-D integration

- **Architecture**
  - Topologies for on-chip and off-chip co-design of power supplies
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